

IN THE CLAIMS

Claims 1-26 (Canceled).

27 (New). A packaged combination memory comprising:
 an integrated non-volatile memory first circuit comprising a first memory type, said first circuit to mass store data;
 an integrated volatile memory circuit to cache and make frequent writes;
 an integrated non-volatile second circuit comprising a second memory type, said second circuit to store both data and code;
 an integrated non-volatile third circuit comprising a third memory type, said third circuit to store code, said first, second, and third memory types all being different from one another;
 a processor die coupled to said first, second, third, and non-volatile memory circuits to store information in a selected one of said circuits; and
 a semiconductor integrated circuit package containing said first, second, third, and non-volatile memory circuits as well as said processor.

28 (New). The memory of claim 27 wherein said first circuit is a polymer memory.

29 (New). The memory of claim 27 wherein said volatile memory circuit is a dynamic random access memory.

30 (New). The memory of claim 27 wherein said second circuit is a phase change memory circuit.

31 (New). The memory of claim 27 wherein said third circuit is a flash memory circuit.

32 (New). The memory of claim 27 including at least two integrated circuit memory die and said processor die within said integrated circuit package.

33 (New). The memory of claim 27 wherein said package includes contacts and said processor is coupled most directly to said contacts.

34 (New). The memory of claim 27 including a polymer memory, a dynamic random access memory, a phase change memory, and a flash memory.

35 (New). A method comprising:
packaging within one integrated circuit package a first circuit comprising a first memory type, said first circuit to mass store data, an integrated volatile memory circuit to cache and make frequent writes, an integrated circuit non-volatile second circuit comprising a second memory type, said second circuit to store both data and code, a third circuit to store code, said first, second, and third circuits all being non-volatile memories and being different from one another; and
forming within said same package, a processor die coupled to said first, second, and third non-volatile memories and said volatile memory such that said processor to store information in a selected one of said circuits.

36 (New). The method of claim 35 including packaging in said package a polymer memory as said first memory type.

37 (New). The method of claim 35 including packaging in said package a dynamic random access memory as said volatile memory circuit.

38 (New). The method of claim 35 including packaging a phase change memory as said second memory type.

39 (New). The method of claim 35 including packaging a flash memory as said third circuit.

40 (New). The method of claim 35 including packaging at least two integrated circuit memory die with said processor die in said package.

41 (New). The method of claim 40 including coupling said memory die to package contacts through said processor die.

42 (New). The method of claim 35 including packaging a polymer phase change and flash memory in said package.